an element isolation insulating film including a first insulating film buried to define active element areas on said semiconductor substrate, and a second insulating film shallower and wider than said first insulating film and positioned over the first insulating film; and

elements formed in said active element areas defined by said element isolation insulating film. --

Please add claim 18 as follows:

-- 18. (New) The device of claim 12, further comprising a contact layer formed underneath the second insulating film, and beside the first insulating film. --

REMARKS

Claims 1-17 are pending in this application. By this Amendment, claims 1 and 13-17 are cancelled without prejudice or disclaimer, claims 6-10 and 12 are amended, and claim 18 is added. Claim 1 stands rejected as being obvious over *Park et al.* (U.S. Pat. No. 5,521,115) in view of the IBM Technical Disclosure Bulletin, 1991, and also stands rejected under the judicially-created doctrine of obviousness-type double patenting in view of U.S. Pat. No. 6,236,079. Claims 2 and 6-10 stand rejected under 35 U.S.C. 103(a) as being obvious over *Park et al.* Claims 3-5 stand rejected under 35 U.S.C. 103(a) as being obvious over *Park et al.* in view of *Ishii* (U.S. Pat. No. 5,250,831). Claim 11 stands rejected under 35 U.S.C. 103(a) as being obvious over *Park et al.* in view of *Bronner et al.* Claim 12 stands rejected under 35 U.S.C. 102(b) as being anticipated by each of *Ushiku et al.* (U.S. Pat. No. 5,675,176) and *Bronner et al.* (U.S. Pat. No. 5,606,188) individually.

Additionally, the title has been objected to as being non-descriptive. By the present amendment, Applicants have amended to title to be more descriptive, and respectfully request withdrawal of this objection.

The Action objected to Figs. 1a, 1b, 2a and 2b for failing to indicate that they depict the prior art. By the attached Request for Approval of Drawing Changes, Applicants have added such a legend to these figures, and respectfully request withdrawal of this objection.

The Action objected to the specification for failing to identify the parent application by patent number. By the present amendment, Applicants have amended the specification to refer to this patent number, and respectfully request withdrawal of this objection.

Turning now to the claims, Applicants initially note that the cancellation of claim 1 has rendered the rejection of this claim moot.

Independent claim 2 recites, among other features, a semiconductor memory device that includes a plurality of transistors formed two by two in each of a plurality of active element areas, such that two transistors share one of source/drain diffusion layers, and the other of the source/drain diffusion layers is positioned over regions of two adjacent trench capacitors, the transistors each having a gate connected to a word line continuous in one direction; and a contact layer for connecting the other of the source/drain diffusion layers of each of the transistors to a capacitor node layer of corresponding one of the trench capacitors. Embodiments of the claim 2 invention advantageously provide a reduced cell size, which allows a greater concentration of elements on a memory device.

In rejecting claim 2, the Action relies entirely on *Park et al.*, which is a reference related to a method of making a double grid substrate plate DRAM cell array. In particular, the Action alleges that *Park et al.* shows a substrate 10, trench capacitors 55, semiconductor layer 32/58, element isolating film 30, transistors 14 sharing one source/drain diffusion region 18, and an

other source/drain diffusion layer 20 with each transistor's gate 16/62 connected to a word line, and a contact layer 26 connecting the other source/drain layer 20 to the node layers and bitline contacts 78. Action, p. 6.

However, and contrary to the allegations in the Action, the *Park et al.* patent fails to teach or suggest the device recited in Applicants' claim 2. As an example, *Park et al.* fails to teach or suggest at least a plurality of transistors formed two by two in each of a plurality of active element areas, such that two transistors share one of source/drain diffusion layers, and the other of the source/drain diffusion layers is positioned over regions of two adjacent trench capacitors, as recited, among other features, in Applicants' claim 2. The Action cites the *Park et al.* node 20 to show the claimed other of the source/drain diffusion layers, but *Park et al.* contains no teaching or suggestion that this node 20 is "positioned over regions of two adjacent trench capacitors," as recited, among other features, in Applicants' claim 2. Indeed, an examination of the *Park et al.* node 20, shown in Fig. 10, reveals that the *Park et al.* node 20 is not located over any region of trench capacitor 55. *Park et al.* expressly recites that "[i]n a manner similar to the prior art, a storage capacitor is formed in a deep trench 22 ***adjacent*** to the storage node 20 ...." *Park et al.*, col. 5, lines 8-10 (emphasis added).

Park et al. fails to teach or suggest the novel claim 2 device, and embodiments of the claim 2 device are able to achieve a greater degree of concentration of cells than the *Park et al.* device. The additional cited references, *Ishii, Bronner et al., Ushiku et al.,* and the IBM TDB, do not overcome the deficiencies identified above with respect to *Park et al.*, and for at least these reasons, Applicants submit that claim 2 distinguishes over the cited art.

Dependent claims 3-11 depend from claim 2, and are allowable for at least the same reasons as claim 2, and further in view of the various advantageous and novel features recited therein. For example, claim 4 recites, among other features, the semiconductor device according

to claim 2, wherein the trench capacitors are each shaped substantially in a square having one side equal to 2F, where F is a minimum processing dimension, the sides of the squares are oriented in two orthogonal directions of the word line and the bit line, and the trench capacitors are arranged at a regular pitch of 2F in the bitline direction, and shifted sequentially at a one-half pitch on adjacent bit lines.

In rejecting dependent claims 4 and 5, the Action relies on *Ishii* to show the features added by these claims. *Ishii* relates generally to a DRAM device having a memory cell array of a divided bit line type, and the Action relies in particular on Figs. 5 and 7 to show square capacitors in various orientations. Even assuming, *arguendo*, that *Ishii* disclosed features as alleged by the Action, and assuming that the alleged combination is proper, the alleged combination of *Park et al.* and *Ishii* still would fail to render obvious the novel devices recited in claims 3, 4 and 5. For example, nowhere does *Ishii* teach or suggest that its trench capacitors are "arranged at a regular pitch of 2F in the bit line direction, and shifted sequentially at a one-half pitch on adjacent bit lines," as recited, among other features, in Applicants' claim 4. Similarly, *Ishii* does not teach or suggest active element areas that "are arranged at a regular pitch in [the] bit line direction and shifted sequentially by a one-quarter pitch on adjacent bit lines, as recited, among other features, in Applicants' novel claim 5.

The only discussion offered in the Action regarding these claimed dimensions is the allegation that it is obvious "to make the dimensions of the trench capacitors equal to the minimum processing dimension...." Action, p. 8. No further specification of "the dimensions" is offered, and the Action says nothing of any teaching, suggestion, or motivation for a capacitor "shaped substantially in a square having one side equal to 2F, where F is a minimum processing dimension," as recited, among other features, in claims 3 and 4.

Furthermore, the Action fails to explain why anyone of ordinary skill would choose to combine the Action's chosen features from the *Ishii* and *Park et al.* patents in the particular manner alleged.

Independent claim 12 recites, among other features, a semiconductor substrate; an element isolation insulating film including a first insulating film buried to define active element areas on the semiconductor substrate, and a second insulating film shallower and wider than the first insulating film and positioned over the first insulating film; and elements formed in the active element areas defined by the element isolation insulating film. The novel claim 12 device allows for an improved semiconductor memory device.

In rejecting independent claim 12, the Action alleges that each and every recited feature is disclosed in each of *Ushiku et al.* and *Bronner et al.* Applicants respectfully submit that amended independent claim 12 distinguishes over each of these references. Regarding *Ushiku et al.*, the Action relies on *Ushiku et al.* first embedding material 3 to show the claimed first insulating film, and second embedding material 6 to show the claimed second insulating film. In *Ushiku et al.*, the first and second embedding materials are chosen based on their coefficients of thermal expansion to generate stress at the first groove to intentionally create a crystal defect, alleviating stress and strain in other regions of the groove. *Ushiku et al.* Abstract, col. 8, lines 24-55. There is no teaching or suggestion that the second embedding material 6 is "shallower and wider" than the first embedding material 3 and "positioned over" the first embedding material 3, as recited in Applicants' amended claim 12. For at least this reason, Applicants submit that amended independent claim 12 distinguishes over *Ushiku et al.*

Applicants also submit that amended independent claim 12 distinguishes over *Bronner et al.*, which was also alleged to anticipate claim 12. In rejecting claim 12, the Action alleges that *Bronner et al.* P+ Layer 18 teaches the claimed first insulating film with P+ Layer 18, while the

Bronner et al. SOI layer 14 teaches the claimed second insulating film. Contrary to the Action's allegations, neither of these layers is an "insulating film," as recited in claim 12. The P+ Layer 18 is expressly stated "to provide a ***wiring*** level for the contacted body." *Bronner et al.*, col. 2, lines 61-64. The term "SOI" refers to "Silicon-on-insulator" (see col. 1, line 14), and *Bronner et al.* states that "[t]he SOI wafer 10 includes a ***silicon*** layer 14, referred to as the SOI layer, positioned on top of an oxide layer 16, referred to as the 'SOI back oxide' or '***insulator***'." Furthermore, even assuming that the SOI layer 14 is a "second insulating film," and assuming that the P+ Layer 18 is a "first insulating film," *Bronner et al.* still fails to teach or suggest that the SOI layer 14 is "shallower and wider than the [P+ Layer 18] and positioned over the [P+ Layer 18]," as would be required under the Action's application of this patent. *Bronner et al.* simply does not anticipate or render obvious the novel claim 12 device.

Furthermore, dependent claims 13 and 18 depend from claim 12, and are allowable for at least the same reasons as claim 12, and further in view of the various advantageous and novel features recited therein. For example, claim 13 further recites a contact layer formed underneath the second insulating film, and beside the first insulating film, while claim 18 recites a contact layer formed underneath the second insulating film, and beside the first insulating film.

For at least the foregoing reasons, it is respectfully submitted that pending claims 1-12 and 18 distinguish over the cited art, and are in condition for allowance. Should the Examiner

believe that further discussion and/or amendment is necessary to place the application in condition for allowance, the Examiner is invited to telephone the Applicants' undersigned representative at the number appearing below.

Respectfully submitted,

#42,402

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Date: March 18, 2002

MARKED-UP VERSION OF AMENDED SPECIFICATION AND CLAIMS

IN THE SPECIFICATION:

The Title has been amended as follows:

DYNAMIC SEMICONDUCTOR MEMORY DEVICE HAVING A TRENCH CAPACITOR AND METHOD OF MANUFACTURING THE SAME

Paragraph beginning at line 6 and ending with line 9 has been amended as follows:

This is a Continuation-In-Part application of U.S. Patent Application Serial No. 08/982,478, filed December 2, 1997, now U.S. Patent No. 6,236,079, the entire contents of which are incorporated herein by reference.

IN THE CLAIMS:

The Claims have been amended as follows:

6. (Amended) The semiconductor memory device according to claim 2, wherein said contact layer is buried such that said contact layer extends through the other of said source/drain diffusion layers to reach said capacitor node layer ~~after said transistors have been formed~~.

7. (Amended) The semiconductor memory device according to claim 2, wherein:

said semiconductor layer comprises a first epitaxially grown layer and a second epitaxially grown layer formed on said first epitaxially grown layer;

said contact layer is formed such that said contact layer is buried in said first epitaxially grown layer to reach said capacitor node layer ~~before said second epitaxially grown layer is formed~~; and

~~said source/drain diffusion layers are formed after said second epitaxially grown layer has been formed, and~~ the other of said source/drain diffusion layers has a bottom surface connected to a top surface of said contact layer.

8. (Amended) The semiconductor memory device according to claim 2, wherein said contact layer is formed such that said contact layer is buried in said semiconductor layer to reach said capacitor node layer ~~before said transistors have been formed~~, and the other of said source/drain diffusion layers is connected to said contact layer through a buried diffusion layer formed in an upper side portion of said contact layer.

9. (Amended) The semiconductor memory device according to claim 2, wherein said contact layer is formed such that said contact layer is buried in said semiconductor layer to reach said capacitor node ~~before said transistors have been formed~~, and the other of said source/drain diffusion layers is connected to a top surface of said contact layer through a connection conductor formed on a surface thereof.

10. (Amended) The semiconductor memory device according to claim 2, wherein:

said semiconductor layer comprises a bulk semiconductor layer of another semiconductor substrate bonded to said semiconductor substrate in which said capacitors are formed, and an epitaxially grown layer formed on said bulk semiconductor layer;

said contact layer is formed such that said contact layer is buried in said bulk semiconductor layer to reach said capacitor node layer ~~before said epitaxially grown layer is formed~~; and

~~said source/drain diffusion layers are formed after said epitaxially grown layer has been formed, and~~ the other of said source/drain diffusion layers has a bottom surface connected to a top surface of said contact layer.

12. (Amended) A semiconductor device comprising:

a semiconductor substrate;

an element isolation insulating film including a first insulating film buried to define active element areas on said semiconductor substrate, and a second insulating film shallower and wider than said first insulating film and positioned over the first insulating film; and

elements formed in said active element areas defined by said element isolation insulating film.